AN10348

PIP212-12M Design Guide

Rev. 02 — 27 April 2007 Application note

Document information

Info	Content
Keywords	PIP212, Point of Load, VRM (Voltage Rectifier Module), buck converter
Abstract	The Philips Intelligent Power PIP212-12M is a fully integrated output stage for high current synchronous buck regulators. The PIP212-12M incorporates the functionality of three devices: a MOSFET driver, a control MOSFET and a synchronous MOSFET. This design guide provides an overview of the PIP212-12M along with design and layout techniques to obtain optimal performance from your solution.

Revision history

Rev	Date	Description
02	20070427	The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Removed all AIS functions.
01	20050113	Initial version

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1. Introduction

The Philips Intelligent Power (PIP) devices are fully integrated solutions for the output stages of high current synchronous buck regulators. The PIP212-12M is targeted for use in switching power supplies, voltage regulators, and point of load converters (on board and module designs). The performance of the PIP212-12M makes it the optimal solution for powering advanced microprocessors, high current Digital Signal Processing (DSP), Double Data Rate (DDR) memory systems and Application-Specific Integrated Circuit (ASIC) devices.

The PIP212-12M consists of a high side (control FET), low side (synchronous FET), and a FET driver. Contained in a single surface mount package with integral heat sink, the fully integrated device greatly simplifies the design and layout of single and multi-phase buck regulators.

The PIP212-12M has been designed with high performance MOSFETs and customized driver for superior efficiencies. The driver has been designed to monitor switching dead time and actively eliminate dead time without allowing the devices to go into cross conduction. Efficiencies of greater than 90 % can be realized due to the optimized internal design.

An extensive feature set allows designers to easily and flexibly adapt this part to their specific requirements without additional circuitry. The feature set includes functionality for sequencing, an onboard regulator for providing 5 V power in 12 V only applications and V_O sense to allow current sense back to the Pulse Width Modulation (PWM) controllers. This feature allows multi-phase current sharing designs.

The integrated design allows the PIP212-12M to be used as the building block of buck regulators capable of greater than 30 A per phase and frequencies of up to 1 MHz per phase with greater power densities than are possible with discrete solutions or previous integrated solutions.

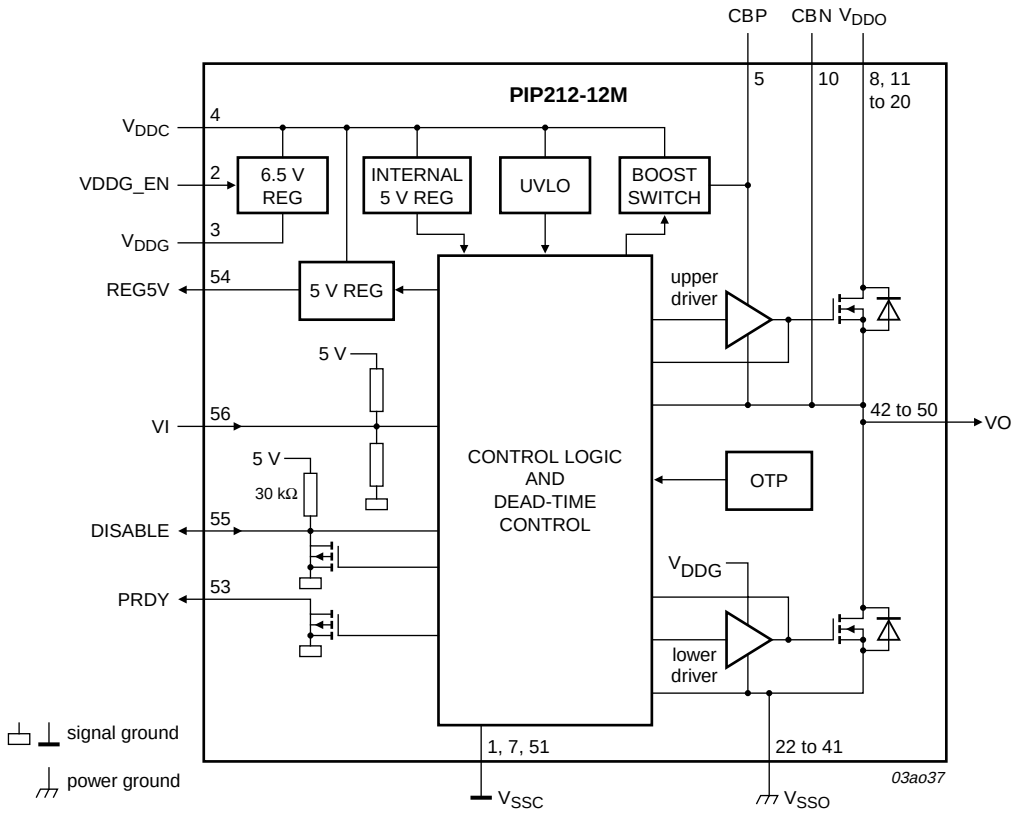


Fig 1. Block diagram of a PIP212-12M

1.1 Typical buck circuit utilizing the PIP212-12M

Using the PIP212-12M device as a building block for a buck regulator requires minimal external components, as can be seen in the typical buck regulator circuit shown in Figure 2. The only additional external components required are the addition of a PWM controller IC, external inductor, input and output capacitors, and a small external boost capacitor.

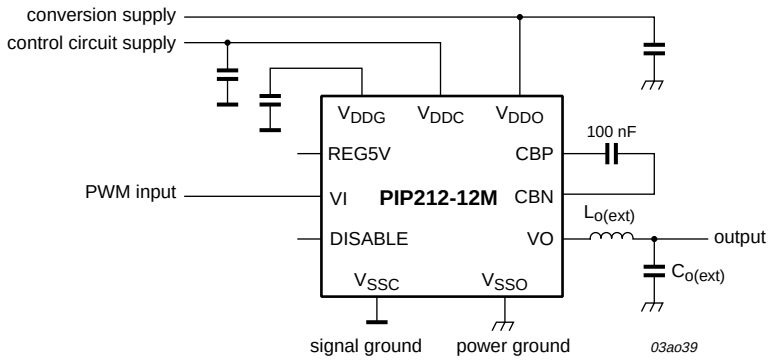


Fig 2. Typical buck regulator circuit using a PIP212-12M

2. Package description and connections

The PIP212-12M is packaged in a low profile ($8 \times 8 \times 0.85$ mm), 56 pin Heatsinked, Very thin, Quad, Flat, No leads, (HVQFN) package. The HVQFN package is the NXP equivalent to the Amkor MicroLeadFrame (MLF) package. The leadless package has 56 perimeter lands (pins) and an additional three separate large pads on the bottom side of the package. The pads (which are electrically connected to many of the 56 perimeter pins) act as large electrical connections to minimize connection impedance for the driver, control FET, and synchronous FET and to provide an excellent thermal connection from junction to Printed Circuit Board (PCB) of less than 4 K/W. The pins and pads that are connected are as follows:

- Driver power ground, V_{SSC}, (PAD 1 and pins 1, 7 and 51)
- Output stage (conversion) power, V_{DDO}, (PAD 2 and pins 8, 11 to 20)
- Output (switch) node, VO, (PAD 3 and pins 42 to 50)

The pad and their corresponding pins should be connected on the layout for optimal electrical and thermal performance. The remaining 56 perimeter lands or pins provide the additional electrical connections required by the PIP212-12M. These pins have been clustered together in groups to provide common high current low inductance electrical connections to the PIP212-12M. For detailed pin descriptions refer to the PIP212-12M data sheet.

The driver power V_{DDC}, and conversion input power, V_{DDO}, are kept separate and have independent ground connections, V_{SSC} and V_{SSO}, respectively. V_{DDC} and V_{DDO} could be provided from the same supply as long as the driver power, V_{DDC} is filtered via an RC network. The driver ground (V_{SSC}) and output stage supply ground (V_{SSO}) must be grounded separately as shown in Section 4 “Layout considerations”.

The PWM input connection, VI, takes a logic level input from any industry standard single or multiphase PWM controller and controls the switching of the control and synchronous FETs. When the PWM signal is HIGH, the control FET is switched on and the synchronous FET is switched off. When the PWM is LOW, the control FET is switched off and the synchronous FET is switched on. A 3-state input (floated PWM output) to VI pin will cause both the control and synchronous FETs to be switched off.

There are several functions available to enhance control, reliability and sequencing:

- UnderVoltage LockOut (UVLO) is implemented internally in the PIP212-12M. The UVLO circuitry monitors the power provided to controller (V_{DDC}). When this voltage is below a certain threshold, operation of the PIP212-12M is disabled. The DISABLE pin is internally held LOW and both MOSFETs are off. The Power-Ready (PRDY) flag indicates the status of the UVLO. The PRDY flag is an open-drain output that is pulled LOW whenever V_{DDC} is below the UVLO threshold. This flag can be used in association with a PWM controller enable function to ensure that the PWM is not enabled until power to the PIP212-12M is good. This is a good way to ensure that the PWM controller does not go through a soft start sequence until all power has come up to adequate levels.
- OverTemperature Protection (OTP) senses the die temperature and will shut down the PIP212-12M in the event that the internal threshold is exceeded. When the external threshold is exceeded, both MOSFETs are turned off and the internal V_{DDG} regulator

is shut down. This functionality protects the PIP212-12M device from being damaged in unexpected operating conditions such as excessive ambient temperatures or if the output currents exceed those intended in the design application.

- The DISABLE pin is used to shut down the PIP212-12M externally. Pulling the DISABLE pin LOW turns off both MOSFETs and disables the REG5V output. The DISABLE pin is pulled HIGH via an internal pull up resistor, but is internally held LOW until the UVLO threshold is exceeded. The PIP212- 12M will enable itself once the UVLO is exceeded as long as an external source does not pull it LOW. In multiphase designs this pin should be connected to all other PIP212-12M DISABLE pins and thus ensure that all PIP212-12M devices remain off until all have exceeded the UVLO threshold; see Figure 3.
- The REG5V function provides a low current regulated 5 V output when both PRDY and DISABLE are HIGH. It can supply power to a PWM controller or as part of an enable function for a PWM controller. Using this pin to power the PWM controller is another way to ensure that the PWM controller does not start-up and go through a soft start sequence until all the PIP212-12Ms are operational.
- The PIP212-12M also features a 3-state input function. If the PWM controller output goes high-impedance, the input to this pin will be driven to nominally 2.5 V by an internal voltage divider. This voltage is between the V_{IH} and the V_{IL} level. If the voltage on this pin remains between these levels for a period longer than the $t_{d(3\text{-state})}$, both MOSFETs are turned off. This function is used by PWM manufacturers to protect against faults such as an overvoltage fault.

2.1 V_{DDG} power options

An external pin, V_{DDG}, is used to supply power to the lower gate drive. The voltage to this pin should be between 5 V and 12 V, and can be adjusted for optimal efficiency depending on the application, as shown in Figure 9 of the PIP212-12M data sheet where V_{DDC} = 12 V, V_{DDO} = 12 V, f_i = 1 MHz, and $I_{O(AV)}$ = 25 A and the optimal value is 6.5 V. In most 12 V applications, a value of 6.5 V will provide optimal efficiency.

For ease of design in applications that do not have access to an external supply, an internal linear regulator will supply this 6.5 V to the V_{DDG}. Leaving the VDDG_EN pin open enables the internal V_{DDG} regulator. If an external supply is to be connected to V_{DDG} then the VDDG_EN pin must be connected to the V_{SSC} to disable the V_{DDG} regulator and a 1 µF capacitor should be connected to the V_{DDG} pin. Note that for minimum power loss, the use of an external 5 V supply is preferred to using the internal V_{DDG} regulator.

3. Multiphase operation

The PIP212-12M device is ideally suited for multiphase operation. The reduced component count and ease of layout make multiphase designs much easier to implement. Efficient high frequency operation minimizes the number of output capacitors required and can also allow replacement of electrolytic capacitors by ceramic capacitors. This reduces the total PCB area required to support large continuous output currents and larger current transients. A typical four-phase solution is shown in Figure 3.

NXP has applied the PIP212-12M in applications from one to four phases and demonstrated currents up to 30 A per phase when converting down from 12 V to 1.2 V at an operating frequency of 500 kHz.

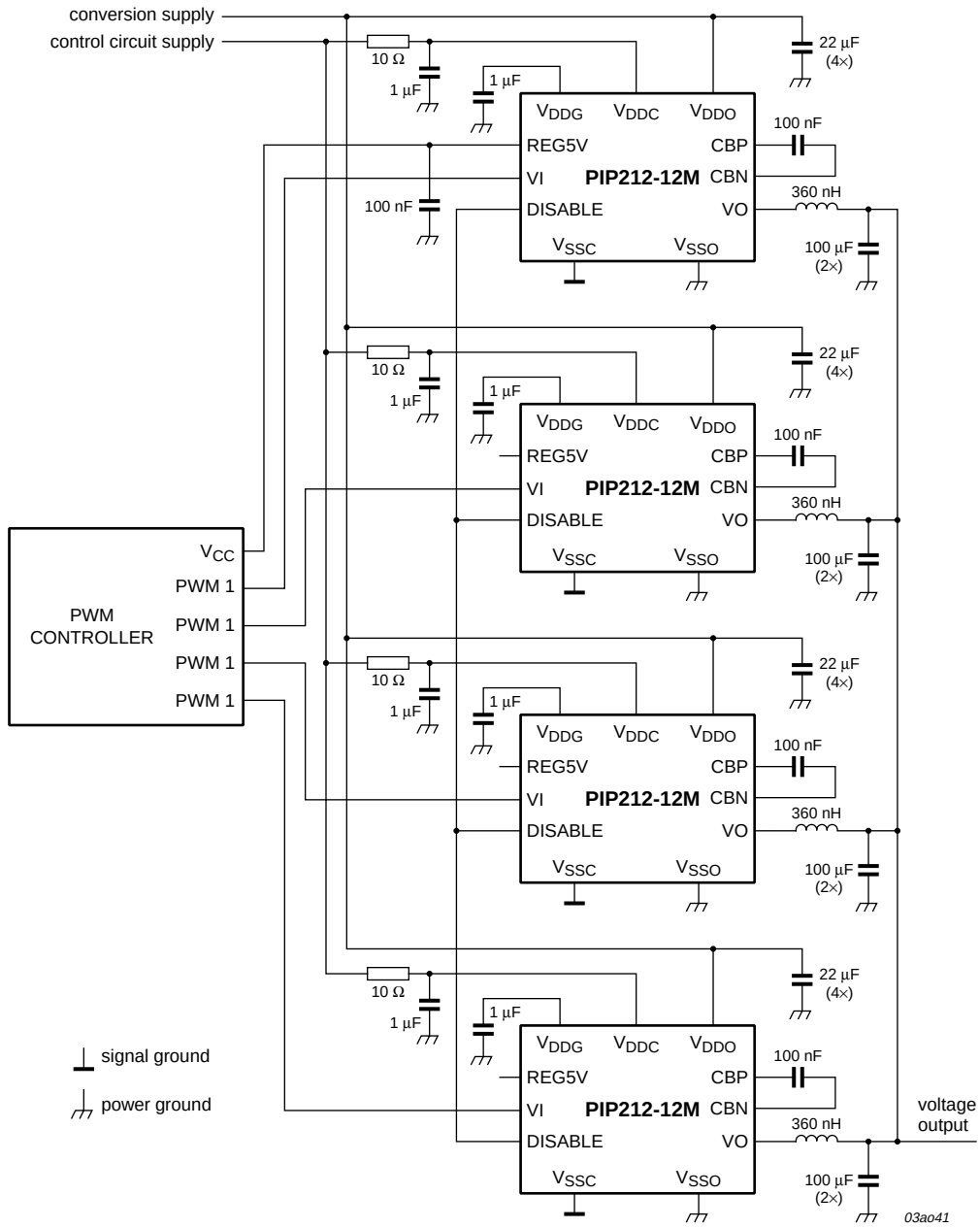


Fig 3. Typical four-phase buck converter circuit capable of 120 A

4. Layout considerations

The PIP212-12M greatly simplifies the layout of a buck converter, as it is a single building block instead of three components (driver, control FET, synchronous FET). For optimal performance, as in any power supply design, a number of elements must be considered when routing the PCB.

4.1 Recommended layout

The 56 perimeter lead lands and three large pads on the package bottom side are rectangular in shape and serve as both electrical and thermal connections. Land patterns corresponding to the pins and pads are made on the PCB and standard re-flow processes are used to solder the package to the motherboard.

In order to take full advantage of the thermal and electrical benefits the HVQFN package has to offer, the PCB should have features to provide adequate power and grounding connections to minimize noise as well as effectively conduct heat away from the device.

4.1.1 Noise and spikes

Noise and spikes are created due to high dI/dt and/or dV/dt occurring in the presence of package and board parasitics. The main areas of concern are therefore:

- V_{DDO} input cap - Control FET (dI/dt)
- Control FET - Switch node (dI/dt)
- Switch node (dV/dt)
- Switch node - sync FET (dI/dt)
- Sync FET - V_{DDO} input Cap (dI/dt)

  This is effectively the switching power path comprising the current loop from the input capacitor through the power MOSFETs and back to the input capacitor. For the high current path, the connections need to be as short and wide as possible to reduce ringing. Eliminating any overlap of these planes with any others reduces capacitive parasitics. Isolation of the V_{DDO} and power Gnd (V_{SSO}) will prevent noise transmission along the planes to the output.

4.1.2 Typical layout

A typical layout of the part is shown in Figure 4 to Figure 11. The images are from a Philips 2-phase demonstration board, and show applicable principles. A few key features of this layout are important to obtain optimal performance from the PIP212-12M.

1. The parasitic inductance of the V_{DDC} power input to the PIP212-12M should be minimized. Placing the V_{DDC} filter capacitor as close as possible to the PIP212-12M and using the widest and shortest possible PCB connections can achieve this. Pin-out of the PIP212-12M facilitates this as shown in Figure 12.
2. The parasitic inductance of the V_{DDO} power input to the PIP212-12M should be minimized. This can be achieved by minimizing the loop length between the V_{DDO} and V_{SSO} connections to the PIP212-12M. Pin-out of the PIP212-12M facilitates this as shown in Figure 12.
3. The parasitic inductance of the boost capacitor loop should be minimized by placing the boost capacitor as close as possible to the PIP212-12M. Pin-out of the PIP212-12M facilitates this as shown in Figure 12.
4. Expand the copper planes to the high current connections (especially the three large pads under the part) as far around the PIP212-12M device as possible. This will reduce the I^2R losses and allow large areas for conductive cooling. Mirror these copper areas as much as possible on the other layers of the board.

5. Incorporating thermal vias on the V_{DDO} and VO main pads on the PCB will also greatly improve the thermal performance. While the thermal pad provides a solderable surface on the top surface of the PCB (to solder the package die pad on the board), thermal vias are needed to provide a thermal path to inner and/or bottom layers of the PCB. An array of thermal vias with a 1.0 mm to 1.2 mm pitch and via diameter of 0.3 mm to 0.33 mm is recommended for the two main pads mentioned above. Solder masking is also required for thermal vias to prevent solder wicking inside the via during reflow, thus taking the solder away from the interface between the package die paddle and thermal pad on the PCB. The solder mask diameter should be 100 microns larger than the via diameter. The vias can be plugged or tented with solder mask, either from the bottom or the top surface of the PCB.
6. In addition to vias under the part, vias in the main copper areas will also allow for heat transfer into the other layers. Care must be taken when adding these vias, as too many vias will tend to reduce the total copper conduction area and increase the I^2R losses in the conduction plane.
7. Fill unused areas and layers with copper to help increase the board s thermal mass and add more conduction area.
8. Use as thick as possible copper layers (1 oz = 35 μm or 2 oz = 70 μm).
9. Maintain adequate distance between heat generating sources. Key heat generating sources in a typical multi-phase buck converter are the output inductors and other PIP212-12M devices. Selecting this distance will require characterizing and understanding the thermal environment on the PCB.

For more information and detailed PCB design, board mounting, and rework guidelines refer to *'Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages'* which can be found on the NXP PIP212-12M web page.

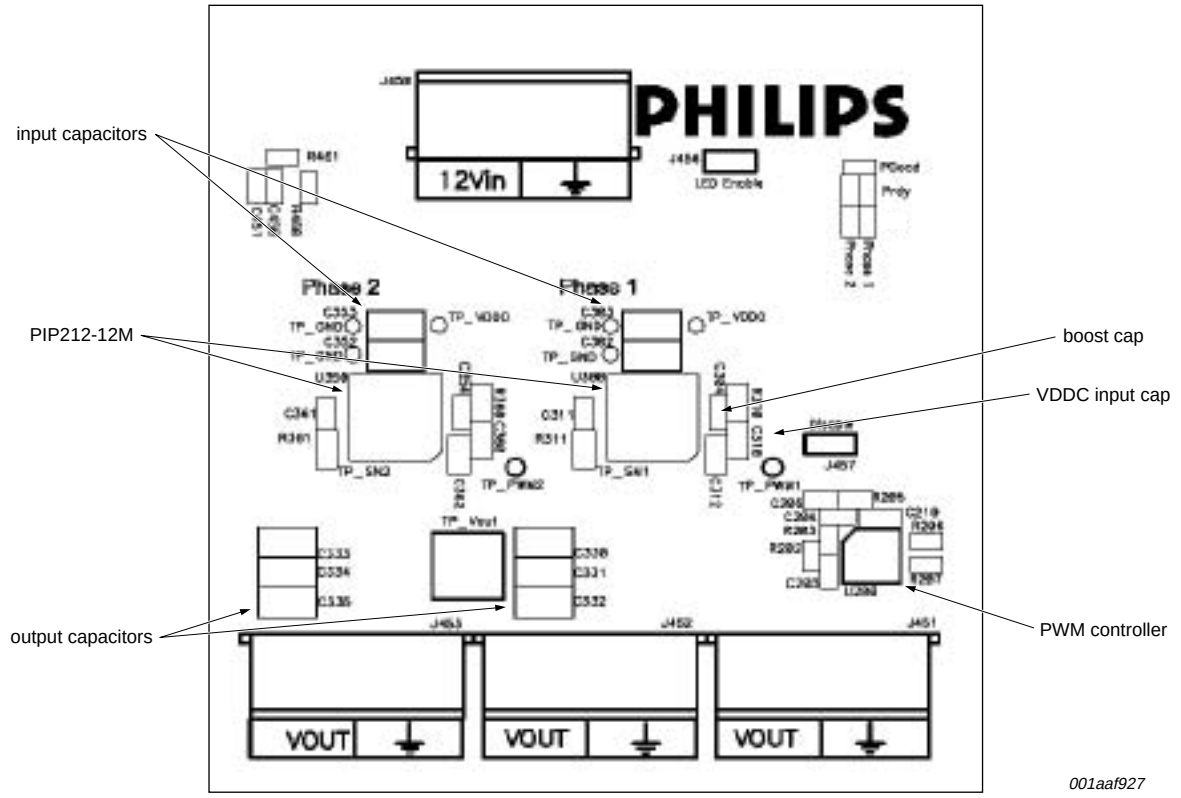


Fig 4. PCB component placement (top view)

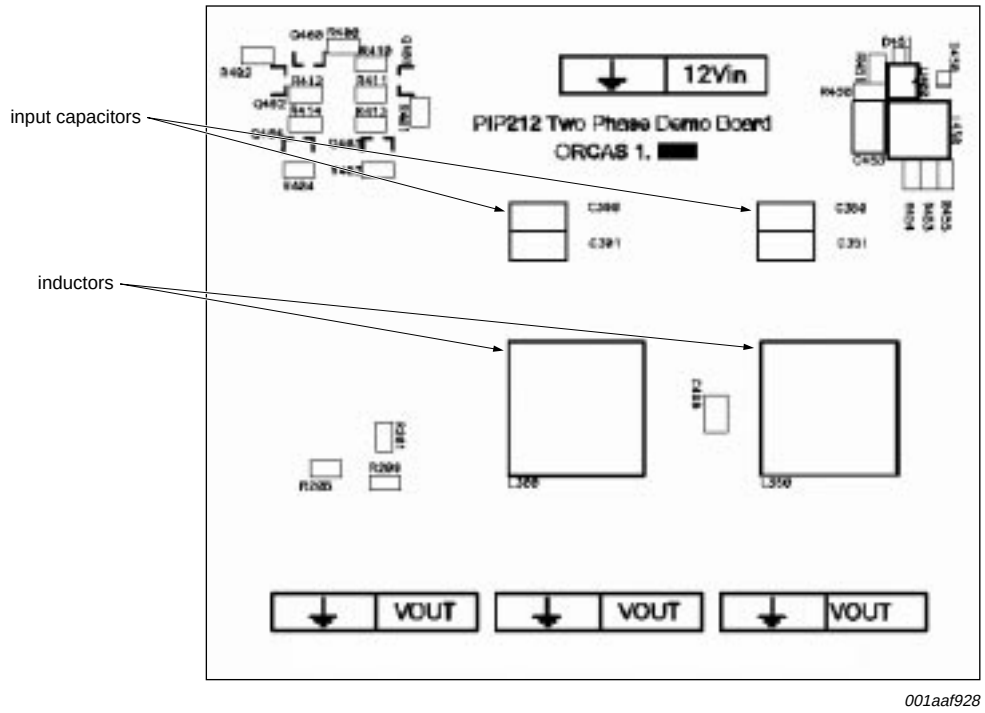
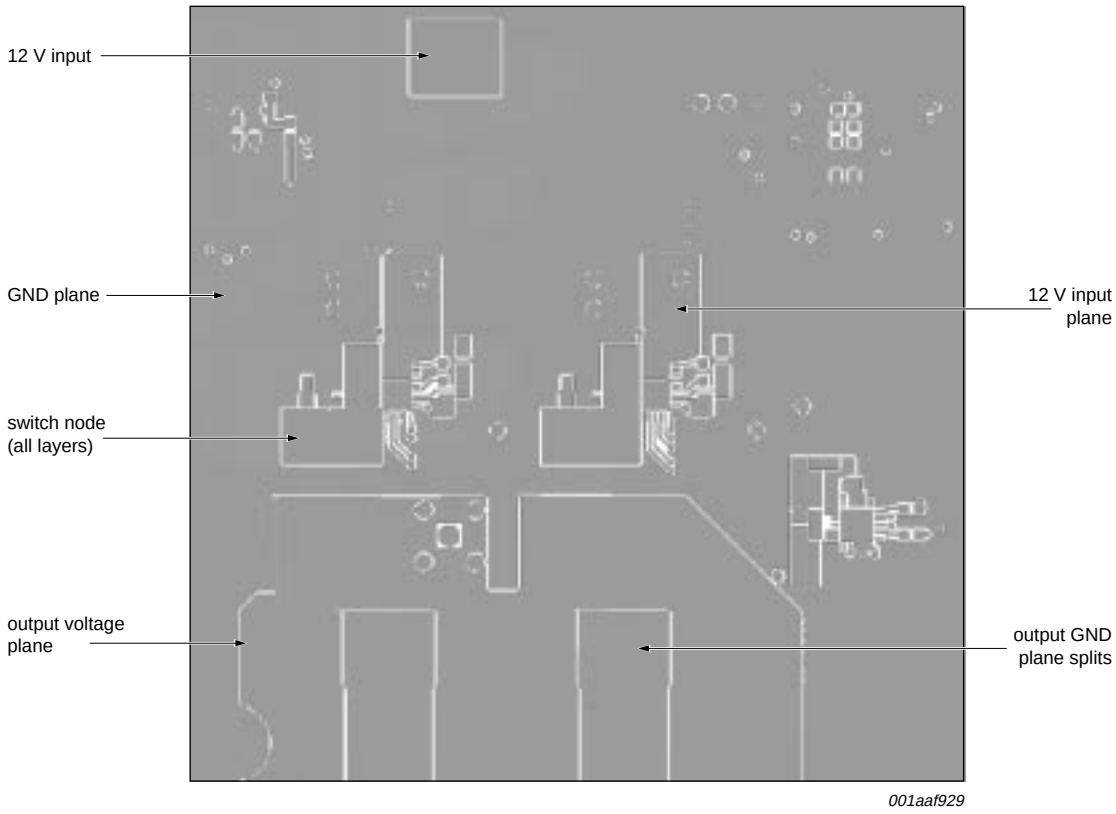
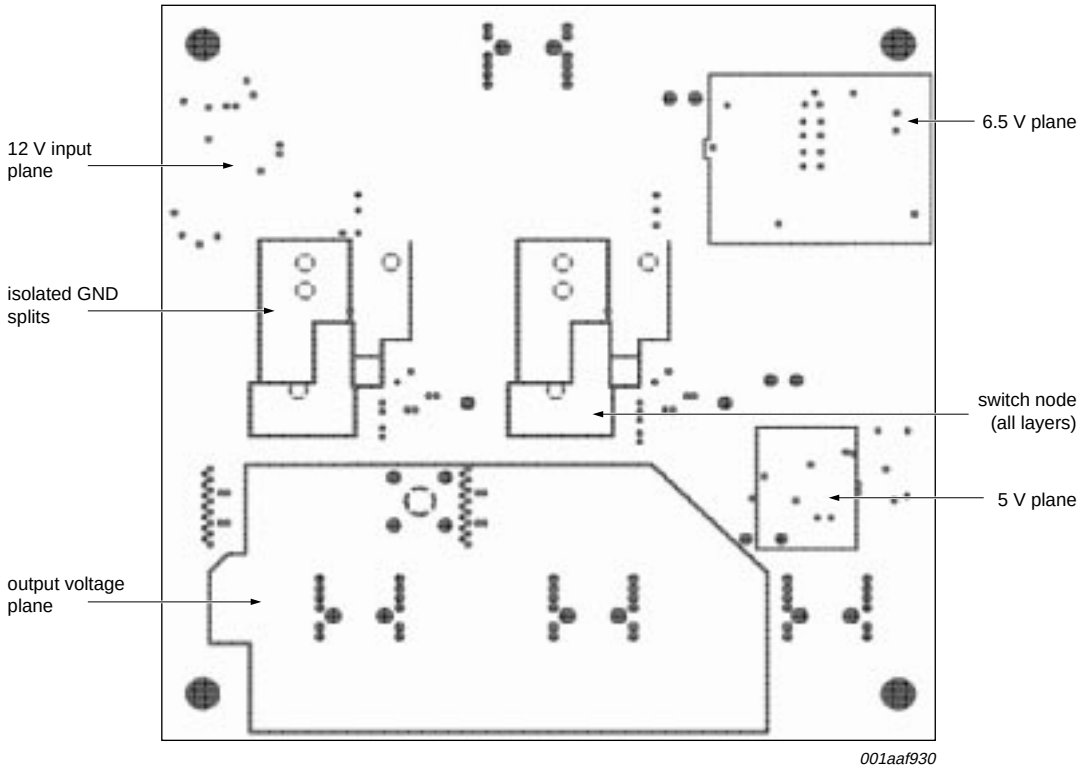


Fig 5. PCB component placement (bottom view)



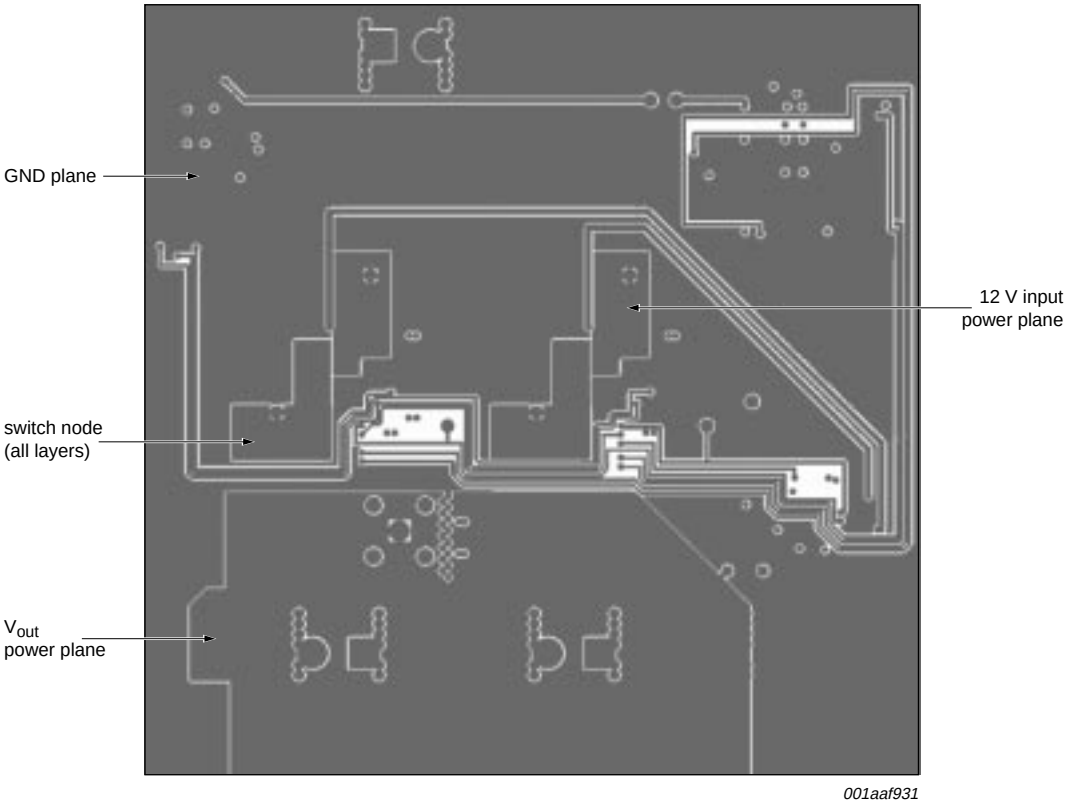
This is primarily a GND plane, with splits for voltage planes. Note the very tight current loops around the PIP212-12M.

Fig 6. Top layer



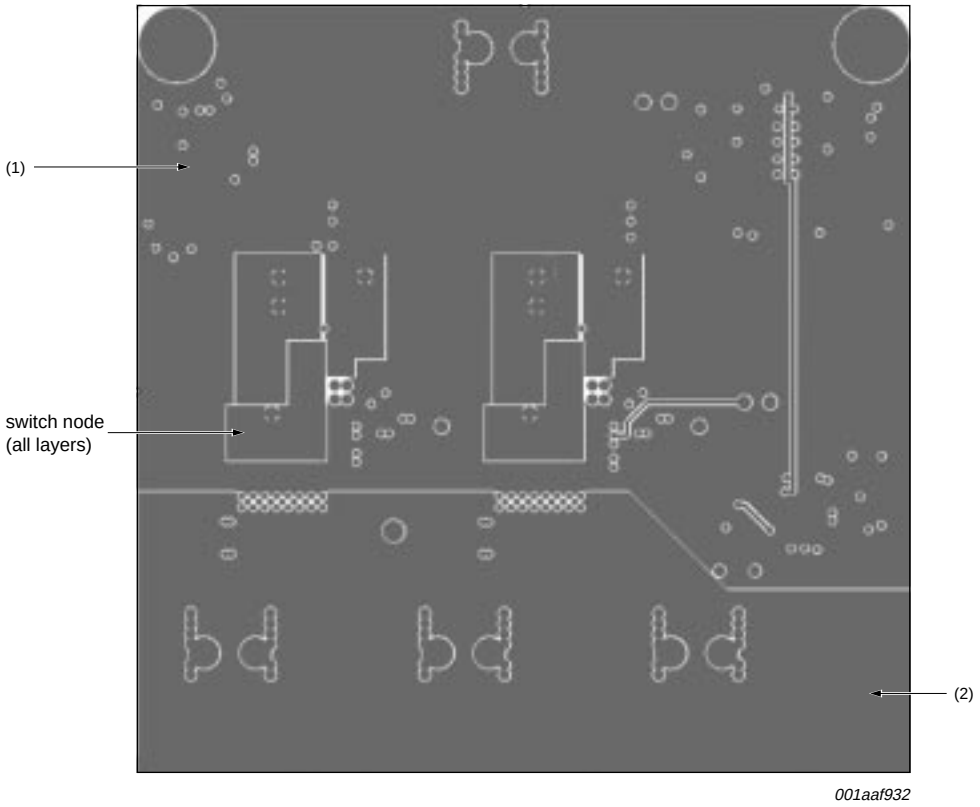
The traces on the power plane are anti-etch and represent plane splits. The white areas are solid copper. Note the very tight current loops around the PIP212-12M.

Fig 7. Power layer



Note that signal and PWM sense lines do not cross over the switching power path loop to ensure the PWM functions properly.

Fig 8. Inner trace layer 1 of PCB, with split GND and V_{out} planes



Note the mirroring of planes from earlier layers.

(1) V_{in} plane with plane splits and isolated GND mounting pads and GND connection.

(2) GND plane with isolated V_{out} vias.

Fig 9. Inner trace layer 2, with split V_{in} and GND planes

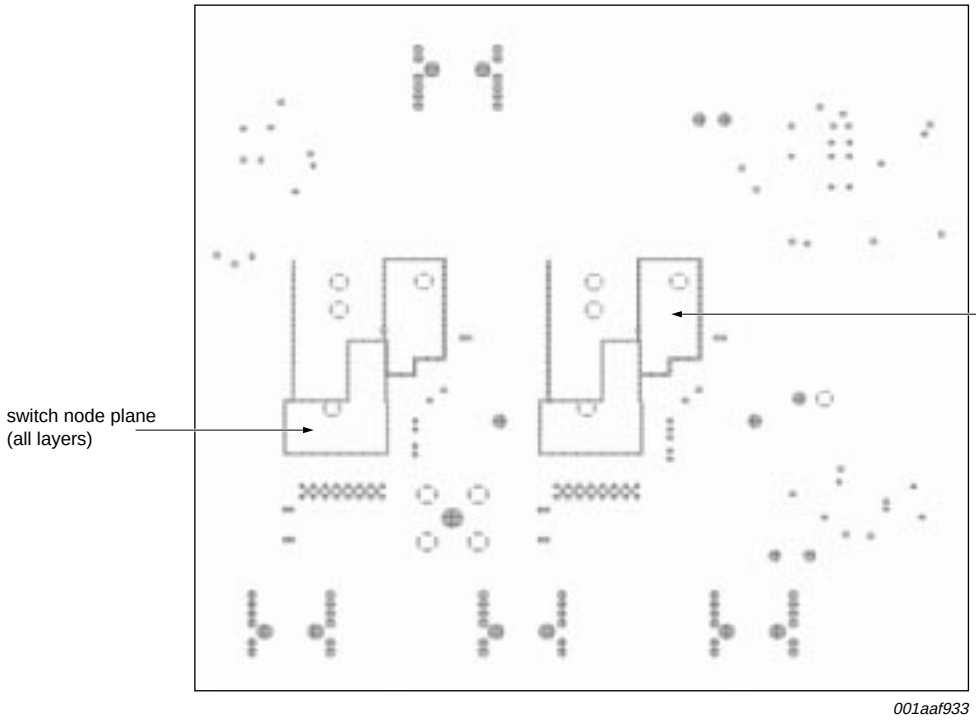


Fig 10. Inner GND plane

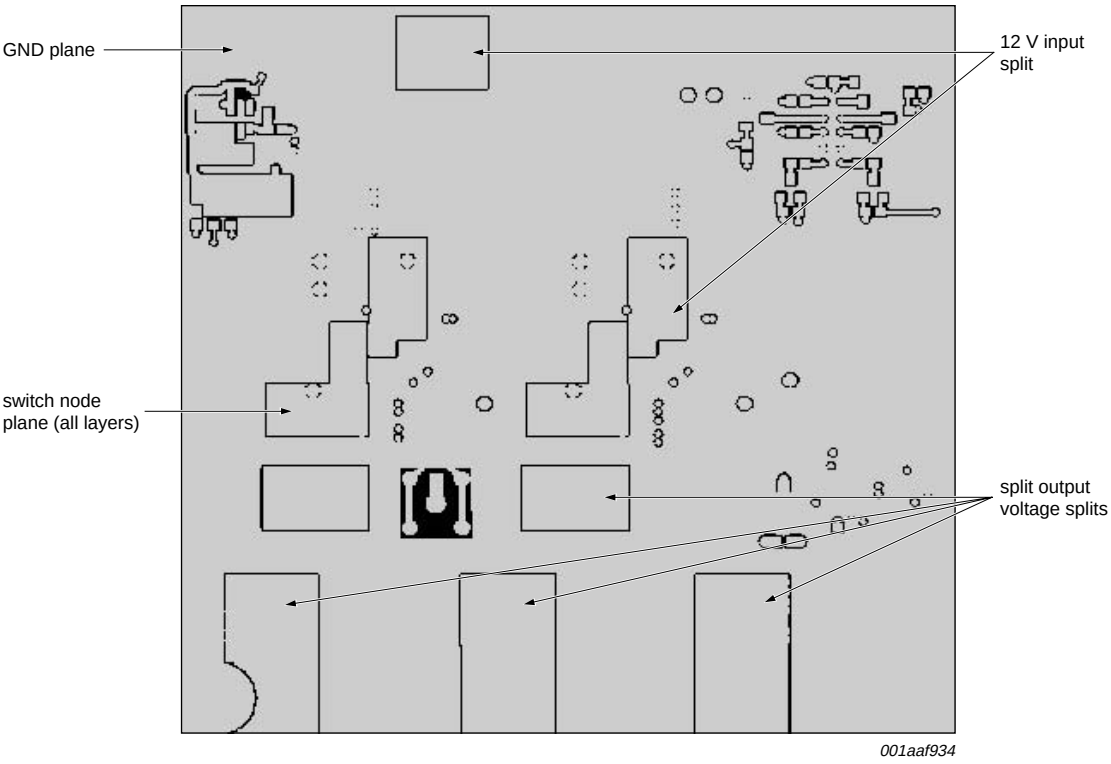


Fig 11. Bottom layer, with voltage plane splits

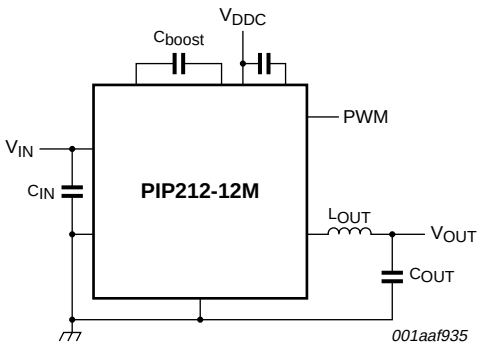
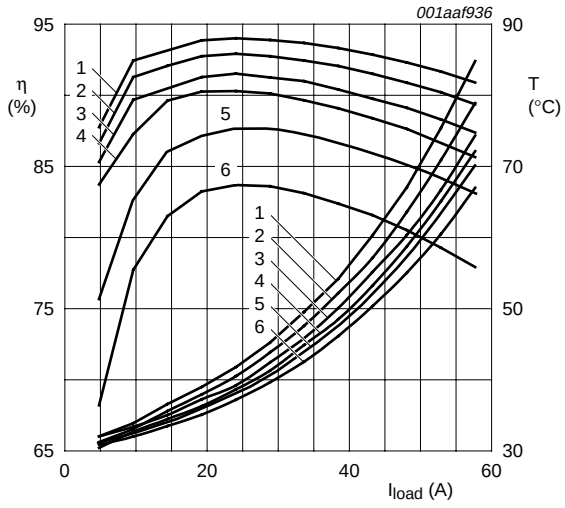


Fig 12. Ease of PCB layout aided by module layout

5. Electrical and thermal performance

The PIP212-12M has been developed to allow designers to easily achieve highly efficient designs. As noted previously, NXP has applied the PIP212-12M in applications from one to four phases. Using layout rules as discussed in the previous section including thermal considerations, Figure 13 shows measured efficiencies and thermal data for a two-phase circuit converting down from 12 V input and operating at 500 kHz per phase, with 200 Linear Feet per Minute (LFM) airflow across the board. The only changes to the circuit to obtain this data were to the voltage divider that established output voltage.



(1) 3.3 V
(2) 2.5 V
(3) 1.8 V
(4) 1.5 V
(5) 1.2 V
(6) 0.8 V

Fig 13. Efficiency and thermal plot for a two-phase circuit at 500 kHz

The thermal environment constrains the maximum performance that can be achieved from a given design solution. Using the Section 4 guidelines on a four layer FR4 board with thermal vias and a minimal foot print of 25 mm × 25 mm copper area, typical junction to ambient thermal resistances of 12 K/W can be achieved.

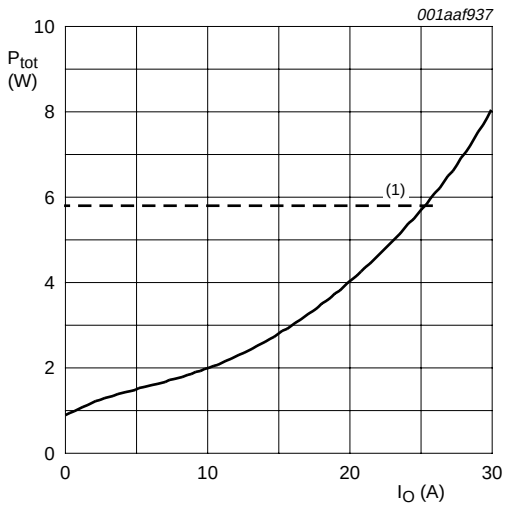
5.1 Typical design and performance

A typical thermal design should make use of the power loss data in the data sheet. To calculate the power loss for a certain set of operating conditions, first determine the power loss for the required output current and then multiply this value by the relevant normalization factor for conditions that deviate from the default conditions used in the PIP212-12M data sheet. The following example describes this process.

For a design with a 12 V input voltage, a 1.5 V output voltage, a switching frequency of 500 kHz and an output current per PIP212-12M of 25 A, the total power dissipation is calculated to be 4.63 W:

$P_{tot} = P_d$ (Figure 14) × F_{Vddo} (Figure 15) × F_{Vo} (Figure 16) × F_{Freq} (Figure 17) × F_{Vddc} (Figure 18) × F_{Vddg} (Figure 19) = 5.8 W × 1.0 × 1.05 × 0.78 × 1.0 × 0.975 = 4.63 W

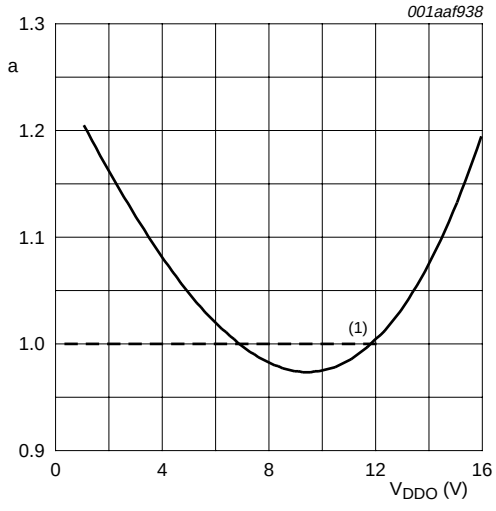
The normalization factors used in the above formula have been taken directly from the data sheet power loss curves, see Figure 14 to Figure 19. These curves are only reproduced for the purposes of this example, please consult the latest PIP212-12M data sheet when calculating power loss.



(1) 5.8 W at 25 A

V_{DDC} = 12 V; V_{DDO} = 12 V; V_O = 1.3 V; f_i = 1 MHz

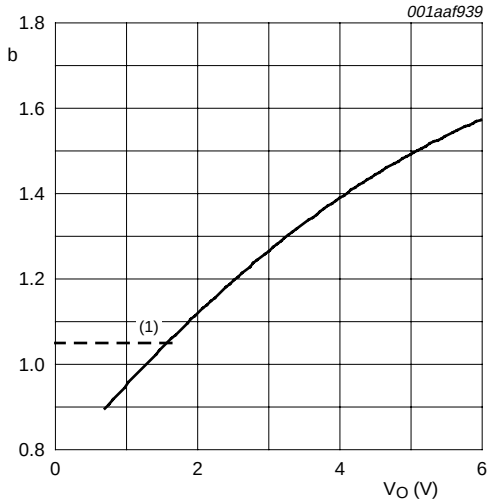
Fig 14. Power dissipated as a function of average output current



(1) 1.0 at 12 V

V_{DDC} = 12 V; V_O = 1.3 V; f_i = 1 MHz; $I_{O(AV)}$ = 25 A

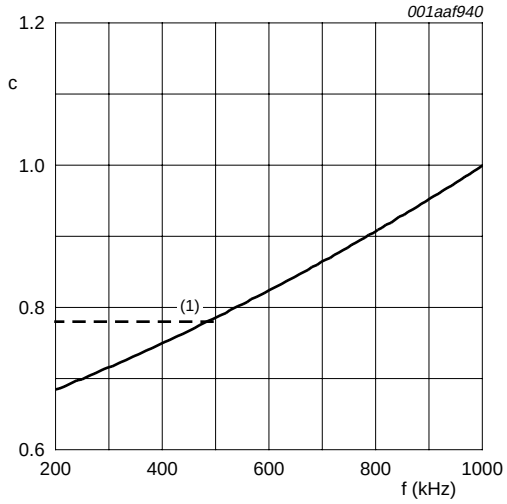
Fig 15. Normalized power dissipation as a function of output stage supply voltage



(1) 1.05 at 1.5 V

V_{DDC} = 12 V; V_{DDO} = 12 V; f_i = 1 MHz; $I_{O(AV)}$ = 25 A

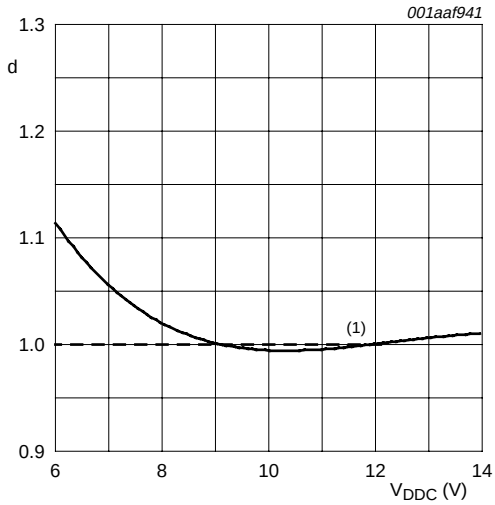
Fig 16. Normalized power dissipation as a function of output voltage



(1) 0.78 at 500 kHz

V_{DDC} = 12 V; V_{DDO} = 12 V; V_O = 1.3 V; $I_{O(AV)}$ = 25 A

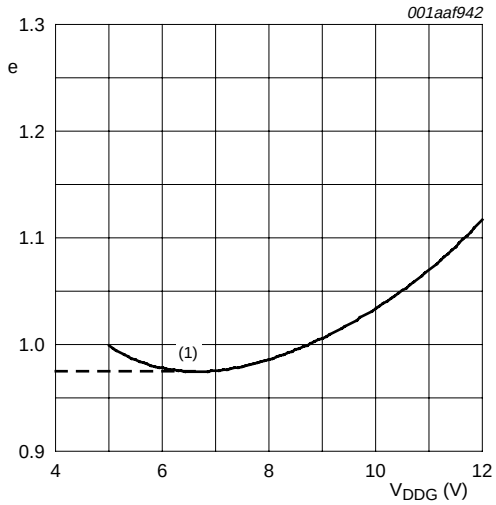
Fig 17. Normalized power dissipation as a function of input frequency



(1) 1.0 at 12 V

V_{DDO} = 12 V; V_O = 1.3 V; f_i = 1 MHz; $I_{O(AV)}$ = 25 A

Fig 18. Normalized power dissipation as a function of control circuit supply voltage



(1) 0.975 at 6.5 V gate drive

V_{DDC} = 12 V; V_{DDO} = 12 V; f_i = 1 MHz; $I_{O(AV)}$ = 25 A

Fig 19. Normalized power dissipation as a function of gate driver supply voltage

6. Summary

The PIP212-12M greatly simplifies the design and layout of the output stage of a buck converter. The small single package allows very dense, low profile designs to be achieved. Integration of the components into a single package reduces the design effort as optimization of the driver and FETs is incorporated as part of the design of the PIP212-12M. The PIP212-12M is also optimized for thermal performance with large underside pads for efficient transfer of heat to the PCB and the thin top plastic coating allowing for easy heat sinking to ambient. The efficient design and superior thermal performance enables high system efficiencies with switching frequencies up to 1 MHz and output currents greater than 30 A. By following a few basic design and layout guidelines, the optimal performance of the PIP212-12M can easily be realized in a design that meets ever-more demanding application requirements.

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